In the REFERENCE TO RELATED APPLICATIONS, please change "08/587,411" to --08/586,411--.

IN THE CLAIMS:

Please cancel claims 49-59, and amend claims 40-48 and enter new claims 60-61 as follows:

40. (Amended) A semiconductor device comprising a [A] field effect transistor having an interface between a semiconductive silicon layer and a gate oxide layer, characterized by post-fabrication passivation of said interface in a heated, deuterium gas-enriched atmosphere at a temperature of [at least] about 200°C to about 1000°C so as to increase the resilience of the field effect transistor to hot electron effects, said post-fabrication passivation being conducted sufficiently to provide to said transistor a practical lifetime at least about ten times that provided by a corresponding passivation with hydrogen, wherein practical lifetime is taken as 20% transconductance degradation as a result of electrical stress.

41. (Amended) The [field effect transistor] semiconductor device of claim 40 wherein said gate oxide layer comprises silicon dioxide.

42. (Amended) The [field effect transistor] semiconductor device of claim 40, wherein said semiconductive silicon layer is a crystalline silicon layer.

43. (Amended) The [field effect transistor] semiconductor device of claim 41, which is an insulated gate field effect transistor, and wherein said post-fabrication passivation is conducted for a period of at least about one hour.

44. (Amended) The [field effect transistor] semiconductor device of claim 43, wherein said semiconductive silicon layer is a crystalline silicon layer.

45. (Amended) The [field effect transistor] semiconductor device of claim 44, wherein said deuterium gas-enriched atmosphere contains from about 0.1% to 100% by volume deuterium gas.

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46. (Amended) The [field effect transistor] semiconductor device of claim 40, comprising deuterium atoms from said post-fabrication passivation covalently bonded at said interface.

47. (Amended) The [field effect transistor] semiconductor device of claim 40, which is encapsulated.

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48. (Amended) The [field effect transistor] semiconductor device of claim 40, which comprises a drain formed in said semiconductive silicon layer, a source formed in said semiconductive silicon layer, a channel extending between the drain and the source, said gate oxide layer over said channel, said interface between said gate oxide layer and said channel, and conductive contacts for said drain, said source and said gate oxide; and

wherein said post-fabrication passivation provides covalently-bound deuterium populating said interface.